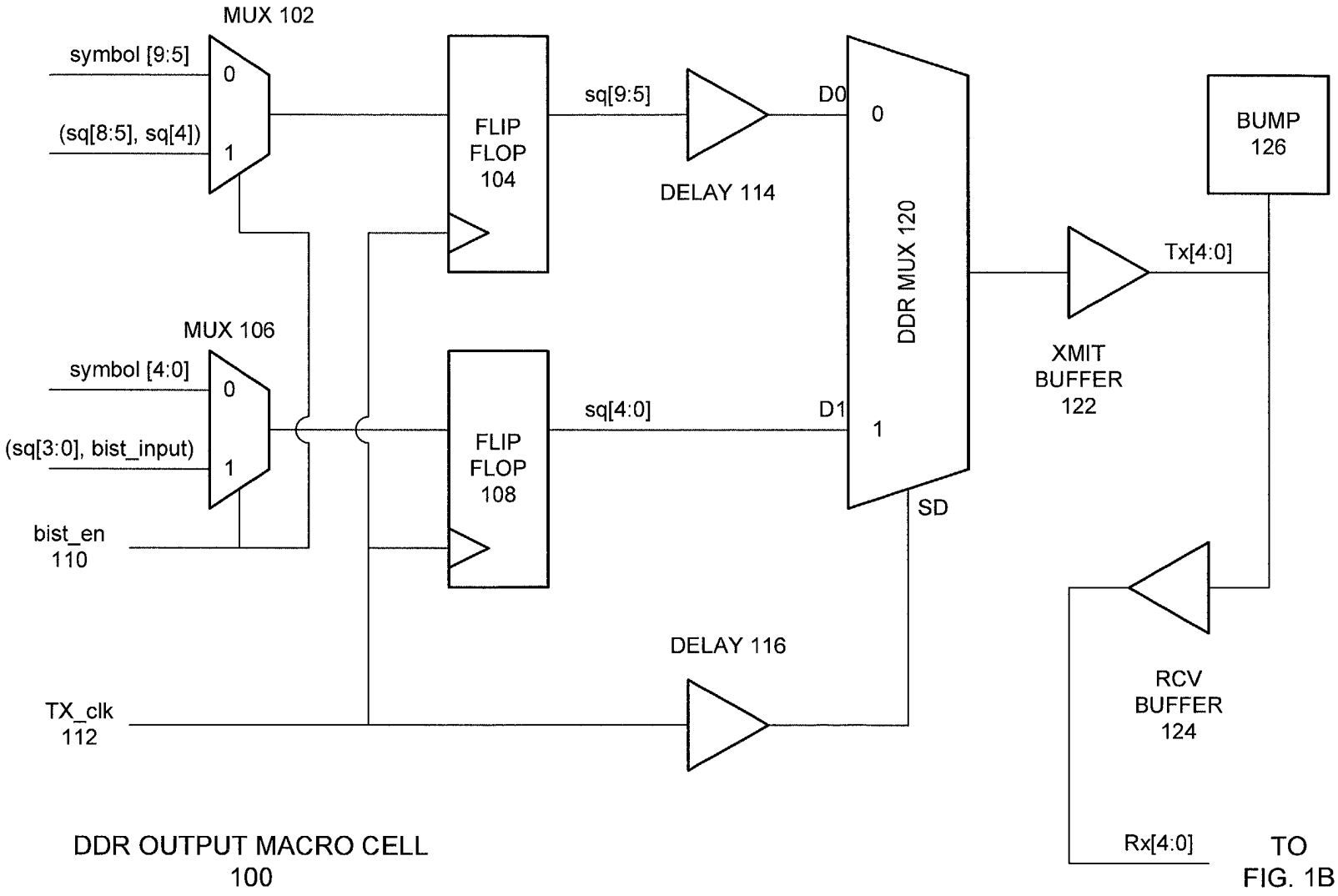
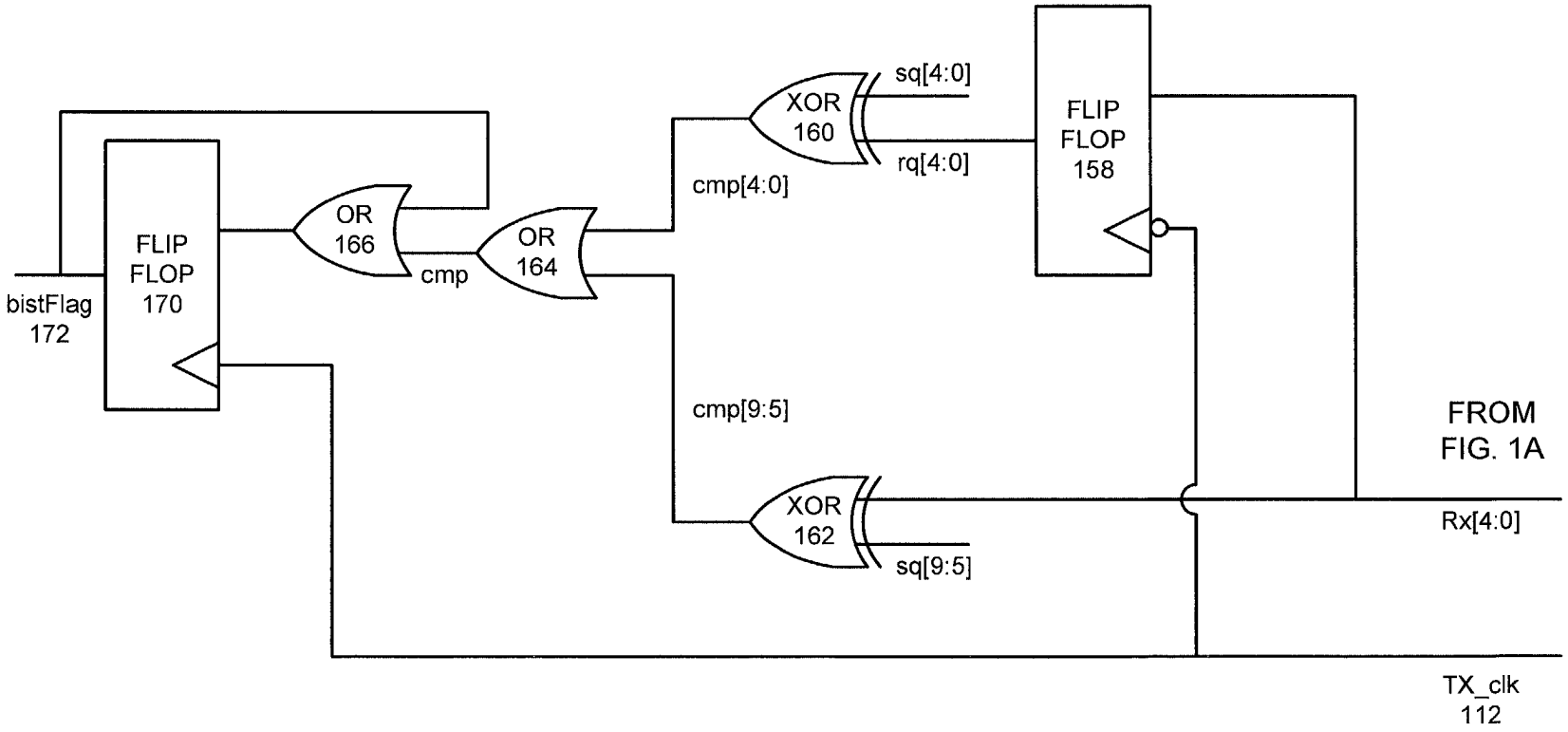
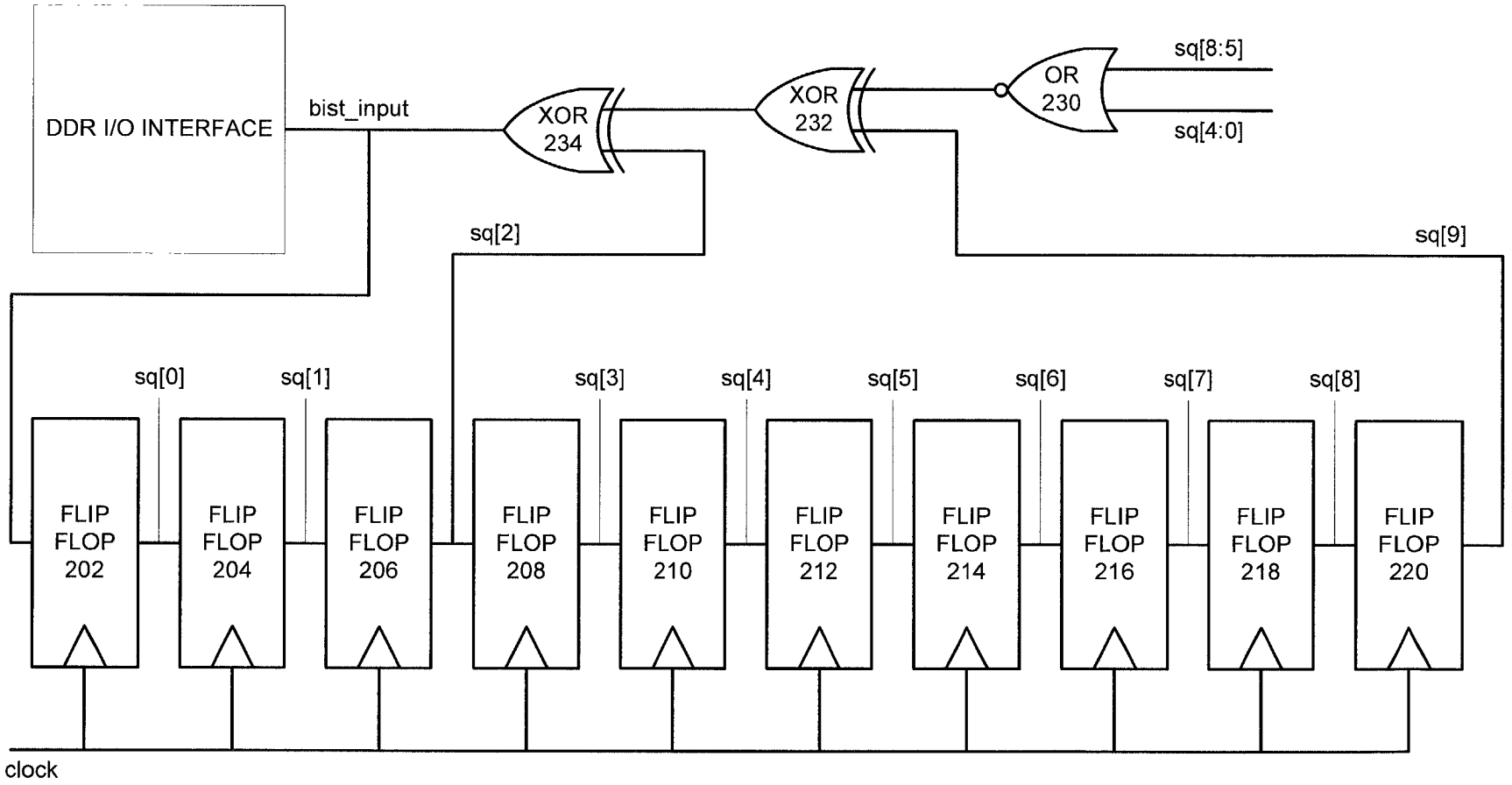

MUX 102
symbol [9:5]
(sq[8:5], sq[4])
0
1
FLIP FLOP 104
sq[9:5]
DELAY 114
D0
0
DDR MUX 120
BUMP 126
Tx[4:0]
XMIT BUFFER 122
MUX 106
symbol [4:0]
(sq[3:0], bist_input)
0
1
bist_en 110
FLIP FLOP 108
sq[4:0]
D1
1
SD
DELAY 116
TX_clk 112
RCV BUFFER 124
Rx[4:0]
TO FIG. 1B
DDR OUTPUT MACRO CELL 100

FIG. 1A



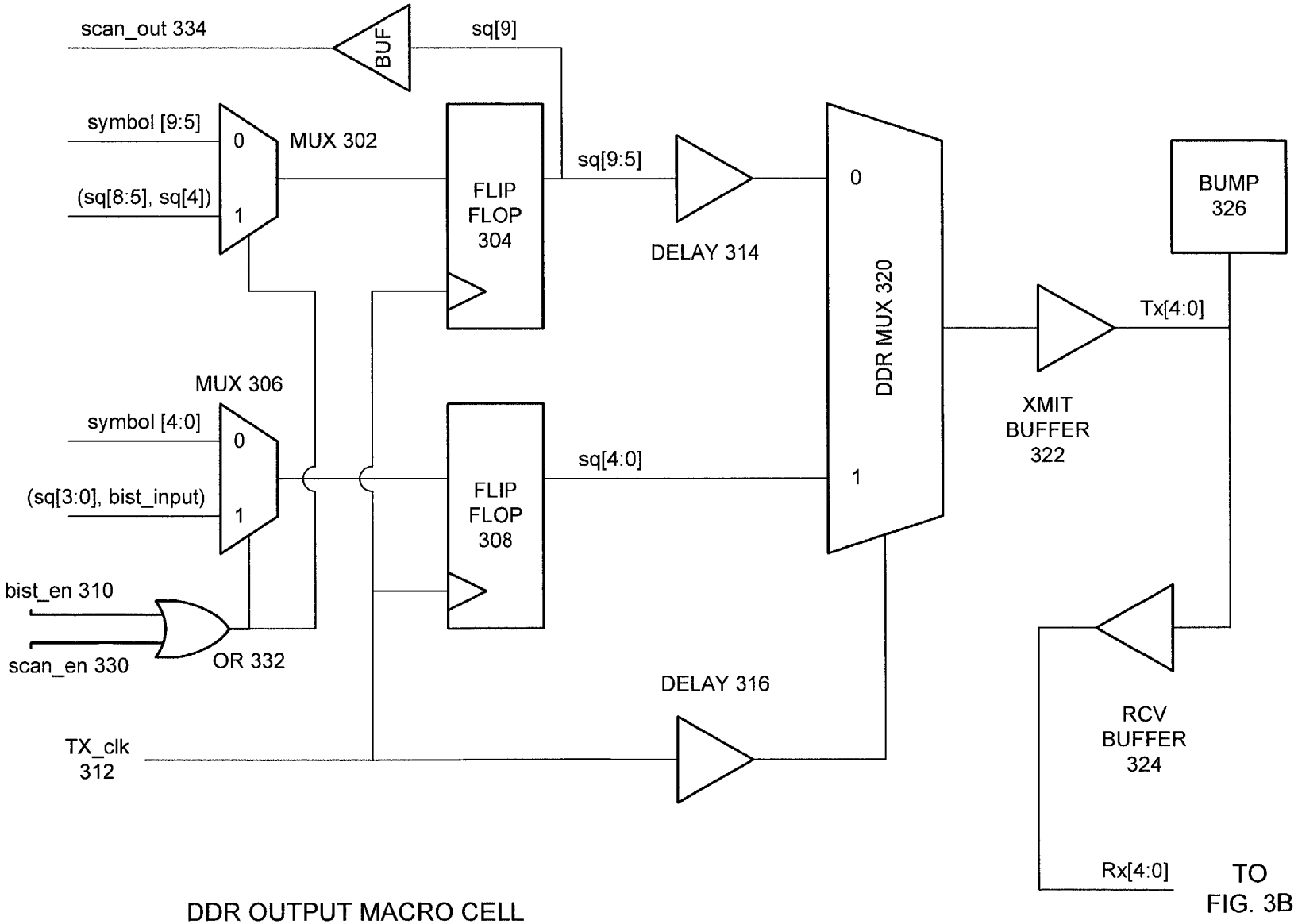
DDR OUTPUT MACRO CELL
100

FIG. 1B



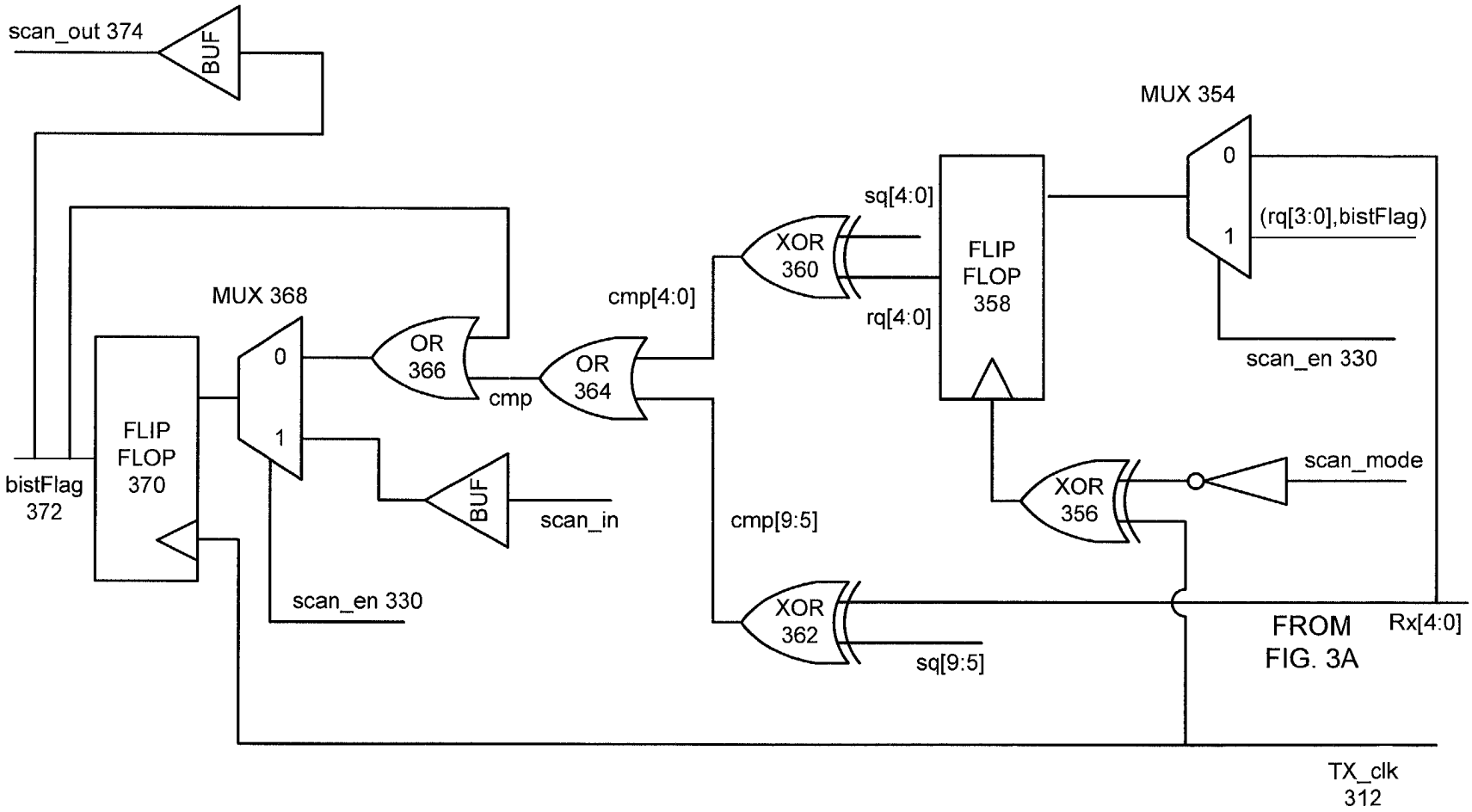
LINEAR FEEDBACK SHIFT REGISTER
200

FIG. 2



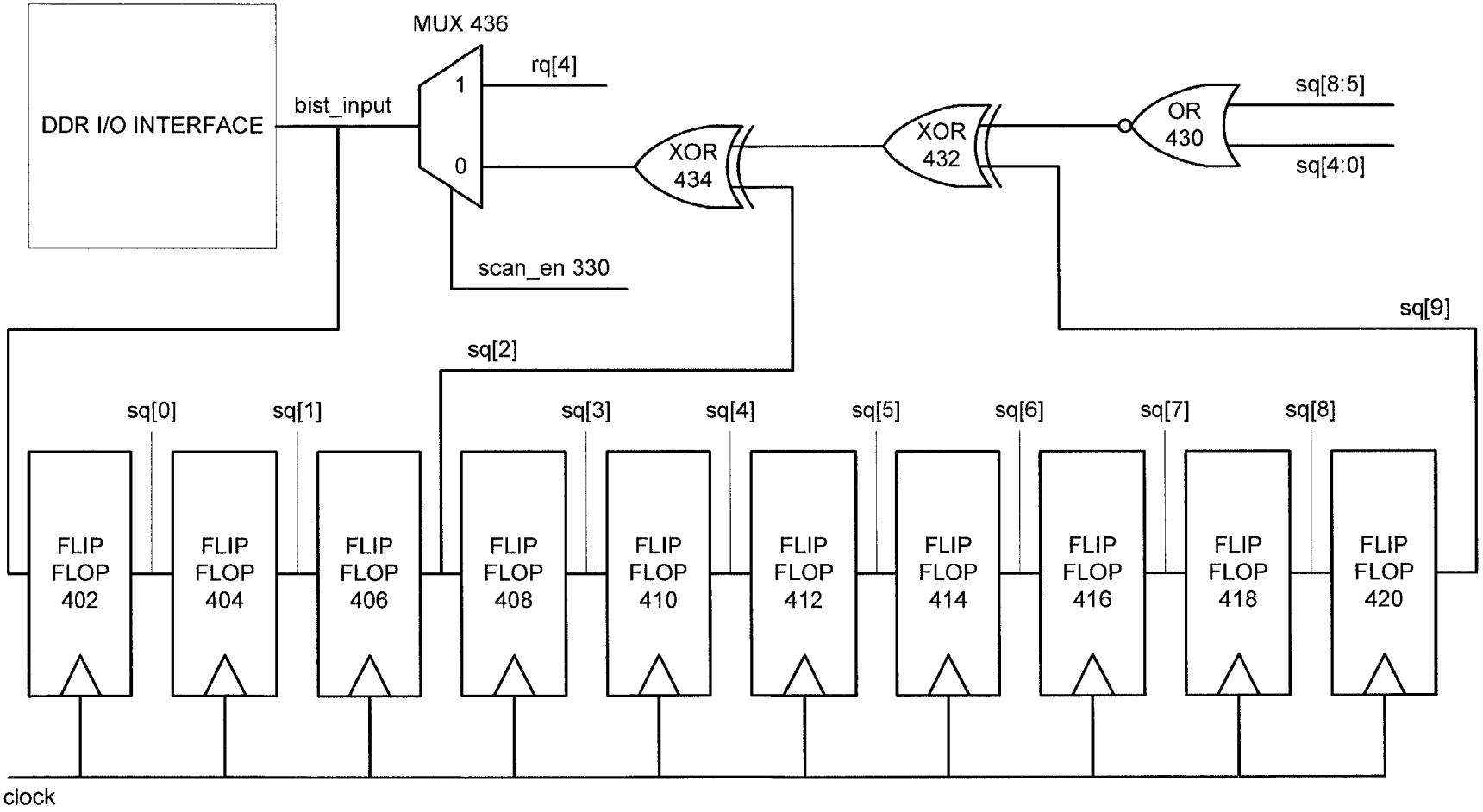
DDR OUTPUT MACRO CELL
300

FIG. 3A



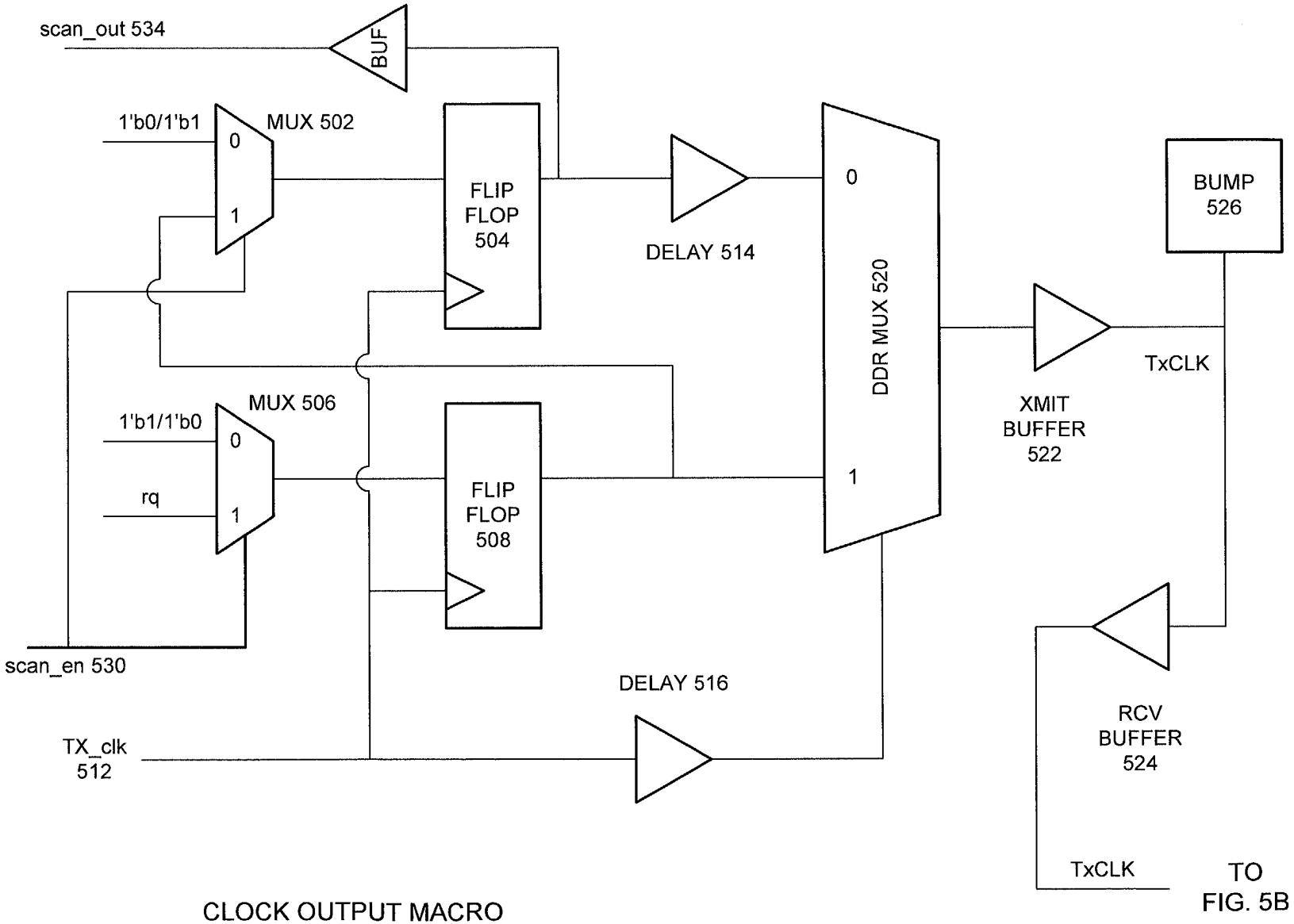
DDR OUTPUT MACRO CELL
300

FIG. 3B



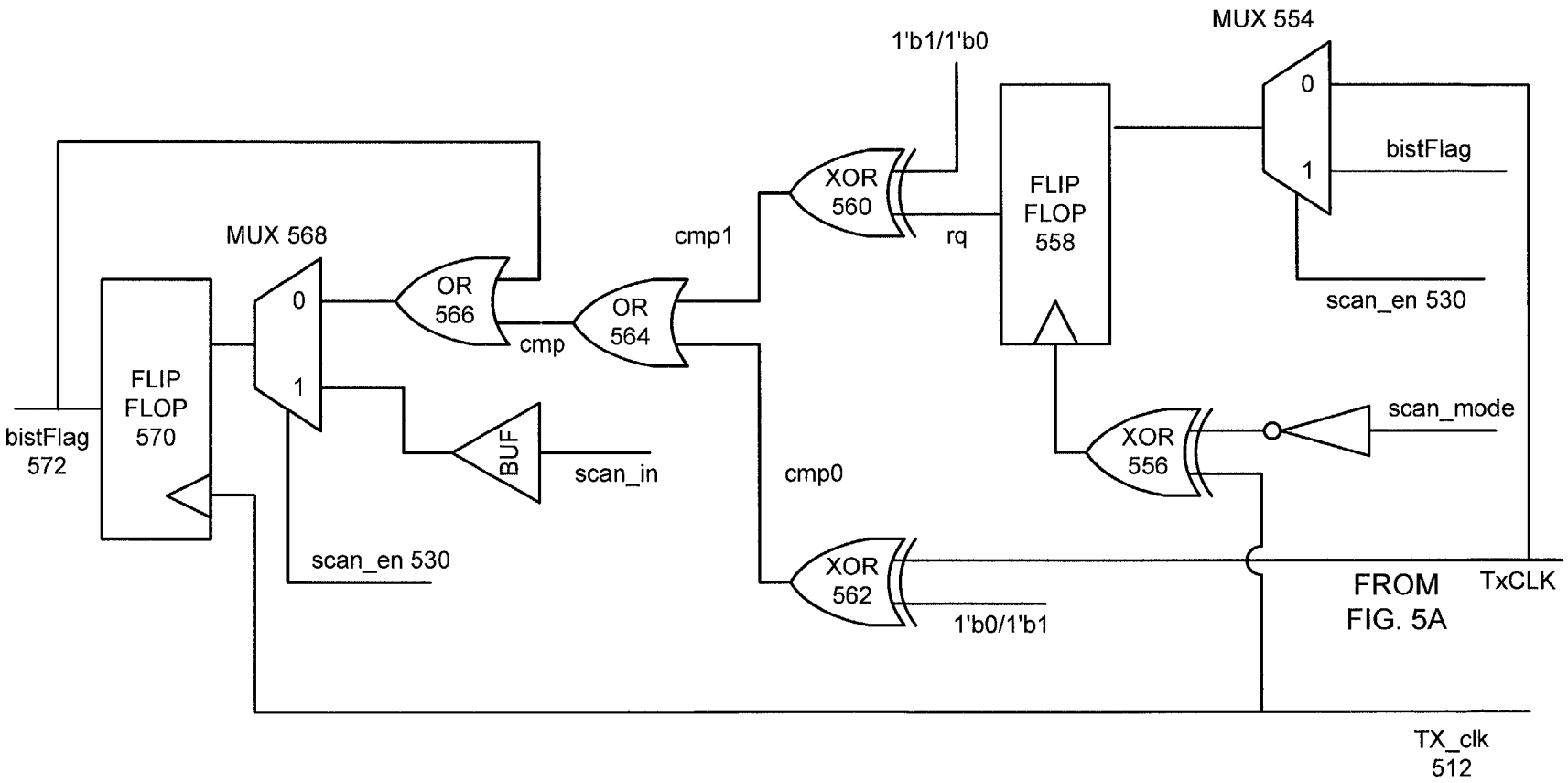
LINEAR FEEDBACK SHIFT REGISTER
400

FIG. 4



CLOCK OUTPUT MACRO CELL 500

FIG. 5A



CLOCK OUTPUT MACRO
CELL 500

FIG. 5B

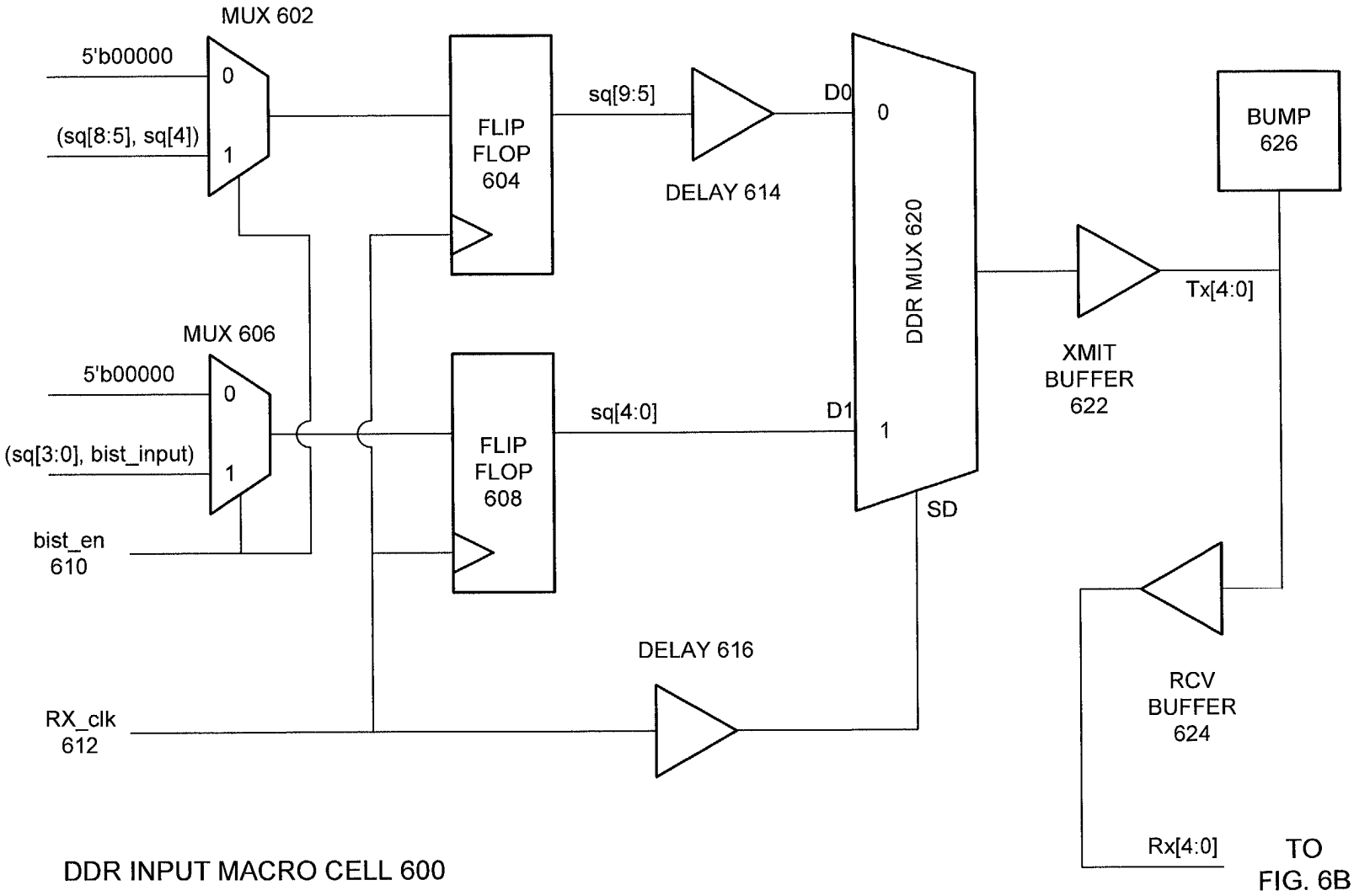
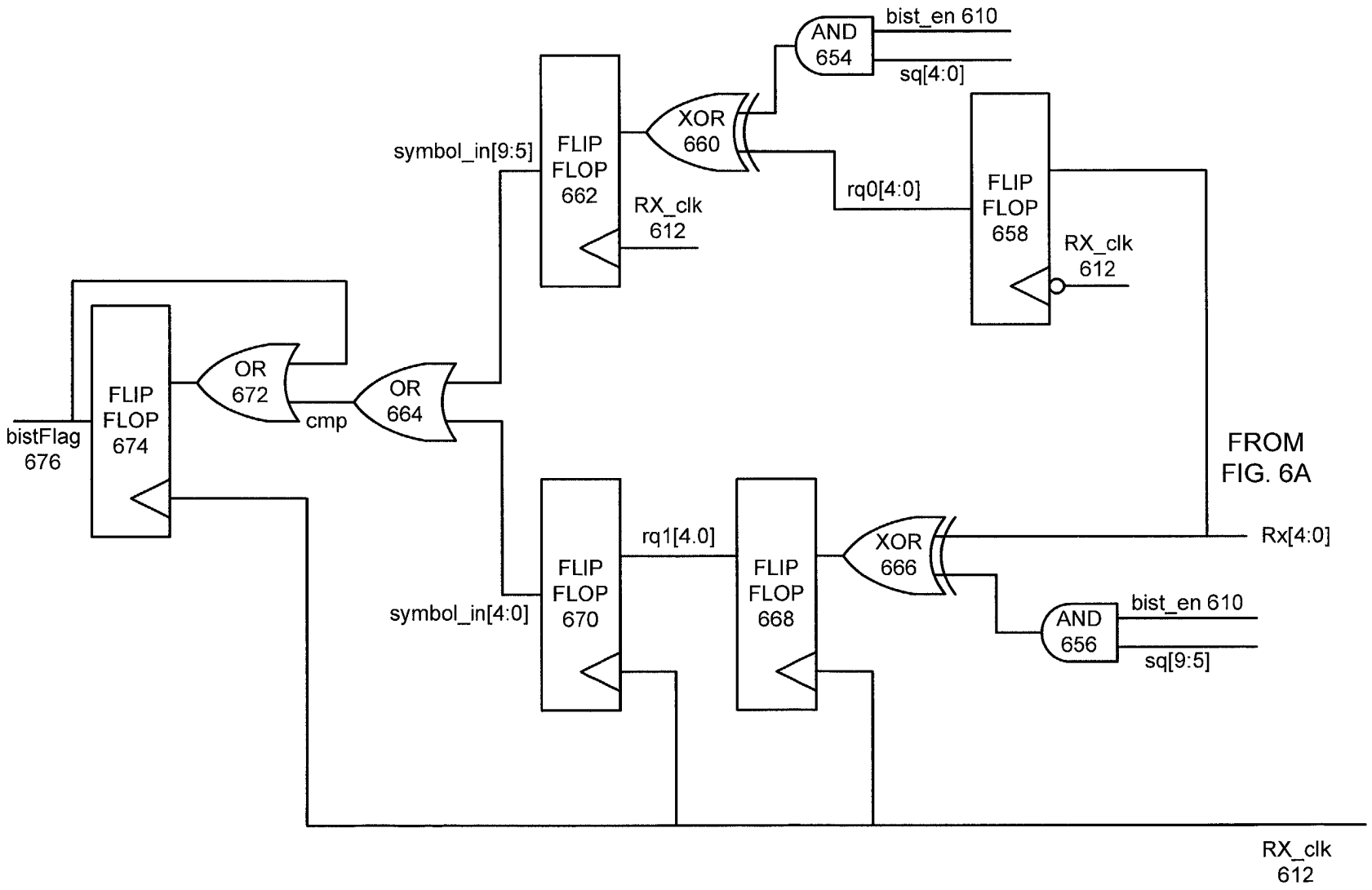

MUX 602
5'b00000
(sq[8:5], sq[4])
0
1
FLIP FLOP 604
sq[9:5]
DELAY 614
D0
0
DDR MUX 620
BUMP 626
XMIT BUFFER 622
Tx[4:0]
MUX 606
5'b00000
(sq[3:0], bist_input)
bist_en 610
FLIP FLOP 608
sq[4:0]
D1
1
SD
DELAY 616
RX_clk 612
RCV BUFFER 624
Rx[4:0]
TO FIG. 6B
DDR INPUT MACRO CELL 600

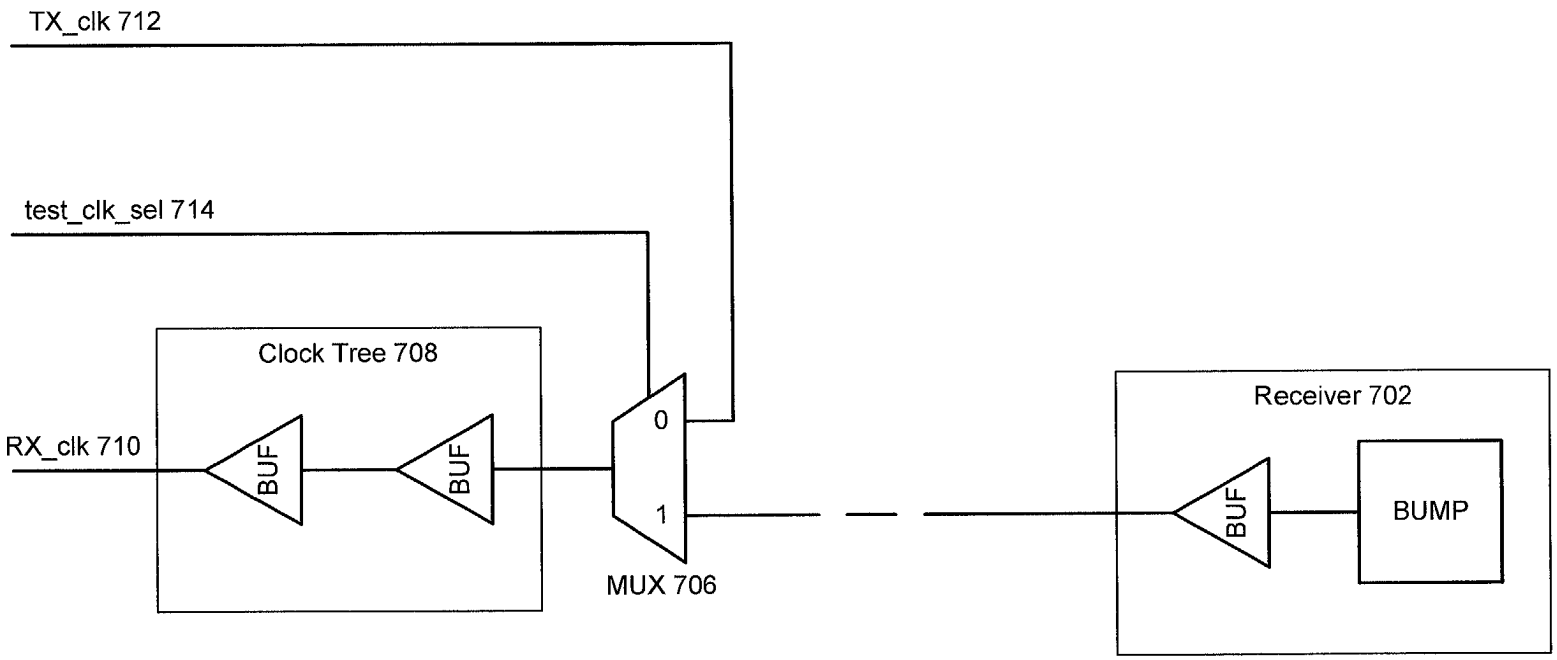
FIG. 6A



DDR INPUT MACRO CELL 600

FIG. 6B

FOZFF 99996660



CLOCK INPUT MACRO CELL
700

FIG. 7

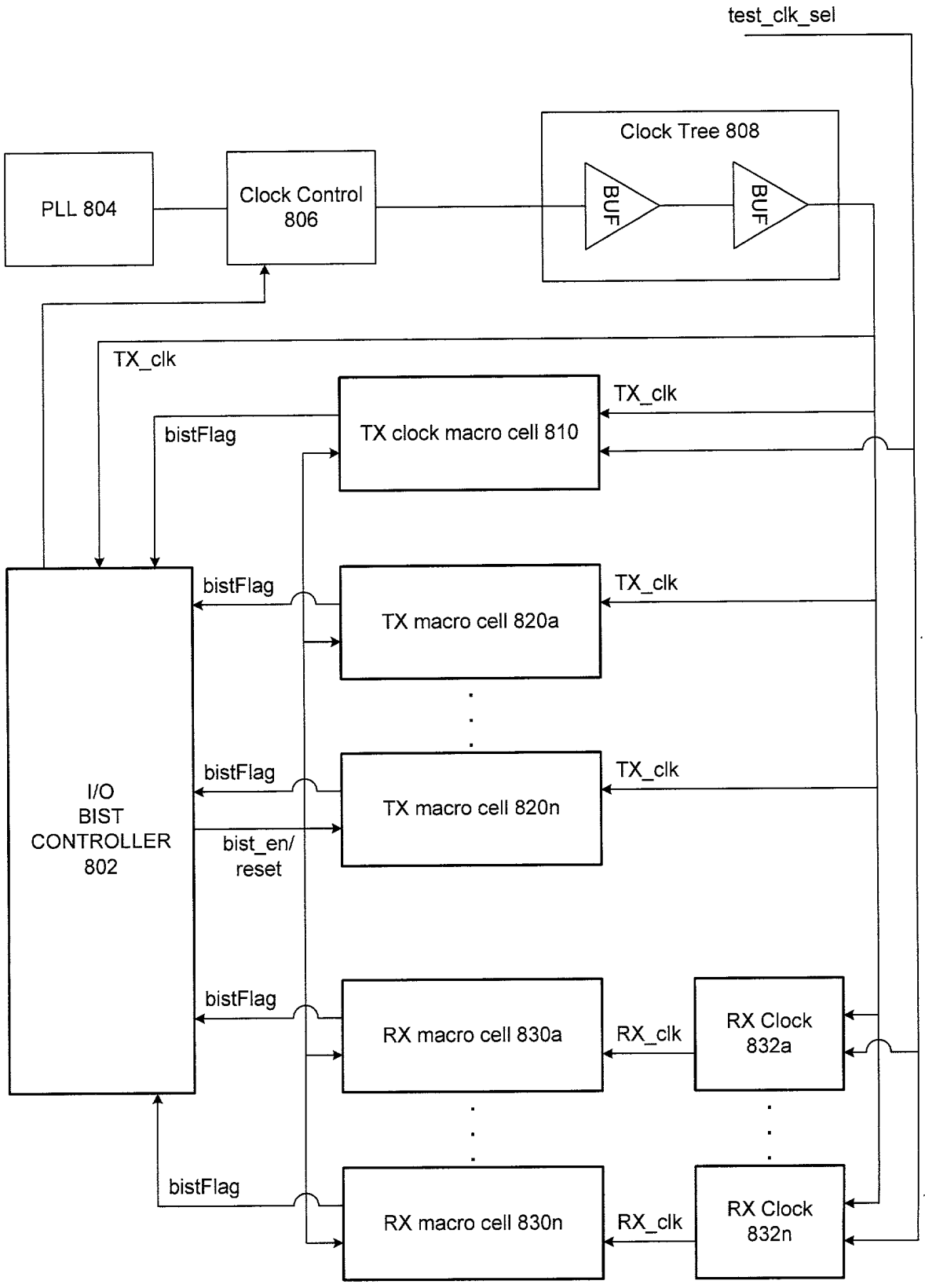

test_clk_sel
Clock Tree 808
PLL 804
Clock Control 806
BUF
BUF
TX_clk
TX_clk
bistFlag
TX clock macro cell 810
bistFlag
TX_clk
TX macro cell 820a
bistFlag
TX_clk
TX macro cell 820n
I/O BIST CONTROLLER 802
bist_en/ reset
bistFlag
RX macro cell 830a
RX_clk
RX Clock 832a
bistFlag
RX macro cell 830n
RX_clk
RX Clock 832n

FIG. 8